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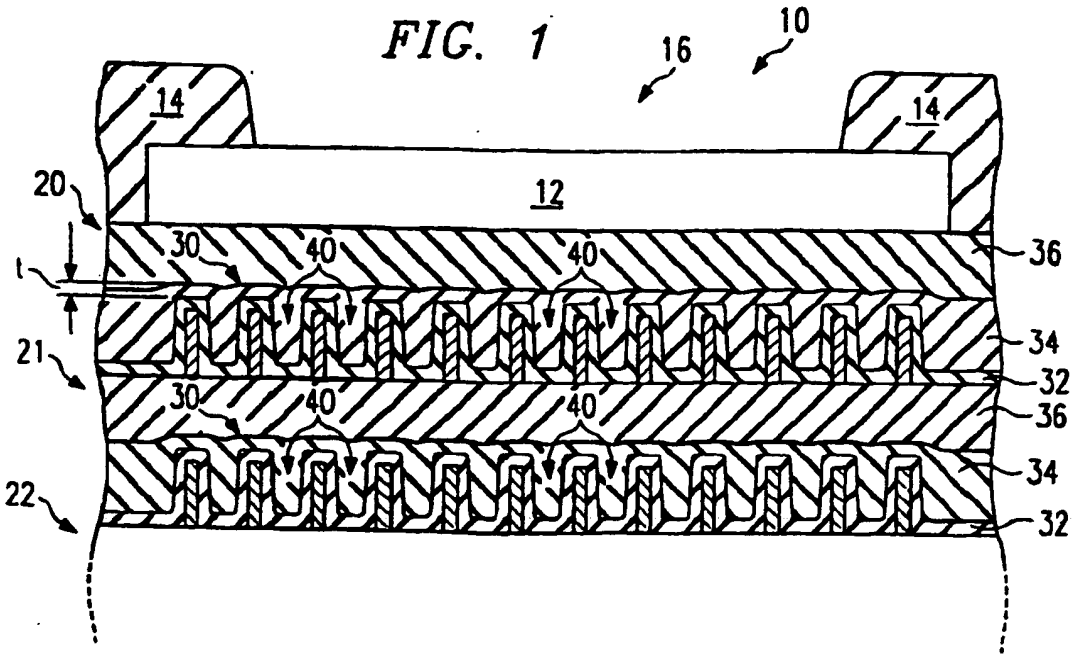
(54) System and method for reinforcing a bond pad

(57) The reinforcing system (10, 70, 90) for a bond pad (12, 72, 92) includes at least one dielectric layer or stack (20, 21, 22, 76, 78, 96, 98) disposed under the bond pad (12, 72, 92). A reinforcing patterned structure (30, 80, 82, 100, 102) is disposed in the dielectric layer or stack (20, 21, 22, 76, 78, 96, 98).

FIG. 1



EP 0 875 934 A2

Description

TECHNICAL FIELD OF THE INVENTION

This invention is related in general to the field of semiconductor devices and processes. More particularly, the invention is related to system and method for reinforcing a bond pad.

BACKGROUND OF THE INVENTION

A well known problem area in semiconductor processing is the process of attaching a solder, wire or other bonding elements to a bond pad on a semiconductor integrated circuit. These bond pads are typically disposed above one or more layers or stacks of brittle and/or soft dielectric materials, typically oxide of silicon and some organic materials, for planarization and insulation purposes. Some dielectric materials, such as hydrogen silsesquioxane (HSQ), aerogels, organic polyimides, and parylenes are advantageous for their low dielectric constants compared to silicon oxides, but are weaker structurally and mechanically.

During the bonding process, mechanical loading and ultrasonic stresses applied by the bonding capillary tip to the bond pad often result in fracture of the underlying dielectrics, deformation of the underlying metal structures, and delamination of the layers in the metal structures. These bonding failures may appear as craters in the bond pad and underlying layers as the bonding capillary tip is pulled away from the bonding pad. However, these defects often are not apparent during bonding but would manifest themselves during subsequent bond pull and shear tests, reliability tests such as thermal cycle or thermal shock, or upon deprocessing and cross-sectioning.

Further, weakness of the bond pad structure may also reveal themselves during wafer probing prior to bonding. Again, the stresses exerted by the probe tips, typically formed of a hard metal such as tungsten, can cause localized fractures in the pads, despite the fact that they make contact with a soft metal (aluminum), on the bond pads. Such fractures are as much of a reliability hazard as those caused during bonding.

Traditionally, the bonding failures have been addressed by altering bonding parameters, such as ultrasonic power and pulse waveform, bonding temperature, bonding time, clamping force, shape of the bonding capillary tip, etc. Much time is spent experimenting with parameter settings and combinations thereof. Although general guidelines of parameter setpoints and configurations have been developed, the bonding failures persist at a sufficiently significant level to continually threaten the reliability of integrated circuit devices. Yet the failure levels are low such that bonding failures become apparent only after several tens of thousands of devices are bonded.

Recent technological advances in semiconductor processing do not alleviate the situation. New dielectric materials with lower dielectric constants are being used to increase circuit speeds but they are mechanically weaker than the conventional plasma enhanced chemical vapor deposition (CVD) dielectrics. Decreasing bond pad dimensions necessitates the increase of vertical bonding force or forces attributable to the use of ultrasonic energy to form effective bonds. Inaccessibility of higher bond parameter settings for fear of damage to the bond pads also results in longer bond formation time, and consequently, lost throughput. All these significant changes point to a trend of more severe failures and increase in their frequency.

SUMMARY OF THE INVENTION

Accordingly, there is a need for a reliable way to prevent or minimize the occurrence of probe and bonding failures where bond pads are situated above one or more structurally and mechanically weak dielectric layers.

In accordance with the present invention, a bond pad reinforcing system and method are provided which eliminate or substantially reduce the disadvantages associated with prior apparatus and methods.

In one aspect of the invention, the reinforcing system for a bond pad includes a reinforcing patterned structure disposed in at least one dielectric stack disposed under the bond pad.

In another aspect of the invention, the reinforcing system for a bond pad includes at least one dielectric layer or a stack of multiple dielectric layers disposed under the bond pad. A reinforcing patterned structure is disposed in at least one dielectric stack.

In yet another aspect of the invention, a method for reinforcing a bond pad in a semiconductor integrated circuit includes the steps of forming a metal layer, patterning the metal layer in a predetermined area into a predetermined pattern having a plurality of vacant areas, and forming a dielectric layer above the patterned metal layer, filling the vacant areas in the patterned metal layer. A bond pad is then formed on the dielectric layer above the patterned metal layer.

In another aspect of the invention, the reinforcing patterned structure may be a joined or interconnected structure. In another aspect of the invention, the reinforcing patterned structure may comprise disjoined or non-interconnected and repeating elements.

A technical advantage of the present invention is the improved structural integrity of bond pads so that forces exerted during bonding and probing do not damage the bond pad and underlying structures. These technical advantages are possible without changing bonding or probing parameters, which may decrease process throughput. The result is a more reliable integrated circuit and decreasing bonding failures.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, reference may be made to the accompanying drawings, in which:

FIGURE 1 is a cross-sectional view of an embodiment of a bond pad reinforcing structure according to the teachings of the present invention;

FIGURE 2 is a plan view of the bond pad reinforcing structure in FIGURE 1 according to the teachings of the present invention;

FIGURE 3 is a cross-sectional view of another embodiment of a bond pad reinforcing structure according to the teachings of the present invention;

FIGURES 4A and 4B are plan views of the bond pad reinforcing structure in FIGURE 3 according to the teachings of the present invention;

FIGURE 5 is a cross-sectional view of another embodiment of a bond pad reinforcing structure according to the teachings of the present invention;

FIGURE 6 is a plan view of the bond pad reinforcing structure in FIGURE 5 according to the teachings of the present invention; and

FIGURES 7-11 are further plan views of varying embodiments of the bond pad reinforcing structure according to the teachings of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Illustrative embodiments of the present invention are illustrated in FIGURES 1-11, like reference numerals being used to refer to like and corresponding parts of the various drawings.

Referring to FIGURE 1, a reinforcing structure 10 for a bond pad 12 is shown. A center portion 16 of bond pad 12 is exposed and uncovered from a protective oxide layer 14 for receiving a ball bond (not shown), typically constructed from aluminum, gold, copper, solder, or like materials. Bond pad 12 is typically a multi-layered stack constructed of aluminum and one or more layers of titanium nitride and titanium, for example. Underlying bond pad 14 is one or more intermetal dieletric layers or one or more dielectric stacks 20-22, each constructed of multiple dielectric layers. Each intermetal dielectric layer or stack 20-22 may include a reinforcing grid 30 disposed in at least one of the intermetal dielectric stacks 20-22. FIGURE 2 shows a plan view of reinforcing grid 30, which has a regular repeating pattern with a plurality of voids or vacant areas.

At least one layer of the intermetal dielectric materials within each dielectric layer or stack 20-22 is constructed of a mechanically and structurally weak dielectric material, such as oxide, hydrogen silsesquioxane (HSQ), Aerogels, organic polyimids, paryl nes, and the like. These dielectric materials are hereinafter referred to generally as weak dielectric materials. Each intermetal dielectric stack 20-22 may include, for example, a first dielectric layer 32, a weak dielectric layer 34, and a second dielectric layer 36. Dielectric layers 32 and 36 may be TEOS (tetraethyl orthosilicate) or any other oxide material formed by a suitable method. It may be seen that by providing a reinforcing structure 30 of a predetermined height, the thickness, t, of weak dielectric layer 34 atop reinforcing structure 30 is greatly reduced. Further, reinforcing structure 30 is a joined or interconnected grid structure with a plurality of voids or vacant areas 40 for containing and accommodating a large portion of weak dielectric material 34 therein. Accordingly, reinforcing structure 30 provides support and mechanical strength to intermetal dielectric stacks 20-22 to substantially decrease the incidents of cratering and other bonding failures caused by wire bonding.

It may be seen from FIGURES 1 and 2 that reinforcing structure 30 is generally planar with a thickness less than the desired thickness of intermetal dielectric stacks 20-22. Further, reinforcing structure 30 is preferably dimensioned to fit generally within and not significantly extending beyond an area defined by bond pad 12. When more than one reinforcing layer is used, reinforcing structure 30 for each intermetal dielectric stack 20-22 may be aligned directly above one another, as shown, or be offset with one another. It is contemplated that any number, including one, of reinforcing structures or layers may be used to achieve improved structural integrity and robustness. It is also contemplated that intermetal dielectric layers or stacks 20-22 may include reinforcing structures of different patterns, although such designs may require additional expense to use different masks to pattern etch the different metal reinforcing structures.

Bond pad reinforcing structure 10 may be constructed by forming a layer of metal or any suitable conductor or semiconductor of predetermined thickness at the start of each intermetal dielectric layer or stack 20-22. The reinforcing layer is then pattern etched into the desired pattern, such as the grid pattern shown in FIGURES 1 and 2. Subsequent dielectric materials are then formed above the patterned reinforcing layer, such as a single dielectric layer or oxide layer 32, weak dielectric layer 34, and oxide layer 36 as shown. Note that weak dielectric layer 34 may be formed by a number of methods, including spin-on, plasma enhanced chemical vapor deposition (CVD), and vapor condensation.

Referring to FIGURES 3, 4A, and 4B, another embodiment of bond pad reinforcing structure 70 is shown. A bond pad 72 is disposed below a protective overcoat of oxide 74 and partially exposed for wire/solder/flip-chip/wedge bonding. Two intermetal dielectric stacks 76 and 78 underlying bond pad 72 include reinforcing structures 80 and 82. Reinforcing structures 80 and 82 include a repeating and non-interconnected pattern such as the crucifix pattern shown arranged in a regular manner. It may be seen that reinforcing structures 80 and 82 may be slightly offset from one another as shown. The semiconductor integrated circuit may include one, two, or more than two intermetal dielectric layers or stacks

with the crucifix reinforcing structure although only two are shown herein.

Yet another embodim nt of the reinforcing structure is shown in FIGURES 5 and 6 in cross-section and plan views, respectively. Int rmetal dielectric stacks 96 and 98 underlie a bond pad 92, which is partially covered by a protective overcoat 94. Intermetal dielectric stacks 96 and 98 include reinforcing structures 100 and 102 respectively. Reinforcing structure 100 in intermetal dielectric stack 96 includes parallel reinforcing lines which are oriented preferably perpendicularly with parallel reinforcing lines of reinforcing structure 102 in intermetal dielectric stack 98. Accordingly, intermetal dielectric stacks in a semiconductor integrated circuit may have reinforcing lines oriented alternately with respect to one another to provide improved mechanical stability and strength. It is further contemplated to provide for reinforcing lines oriented in a manner other than 90 in alternating layers.

Referring to FIGURE 7, an alternate embodiment 110 of the present invention is shown. Reinforcing structure pattern 110 includes reinforcing lines forming a plurality of interconnected or unconnected nested rectangles or squares underlying the bond pad.

FIGURE 8 shows yet another alternate embodiment 112 of possible reinforcing patterns. Reinforcing structure 112 may include a plurality of nested unconnected circles or ellipses underlying the bond pad, as shown. A variation on the nested circle structure 112 is an interconnected or crosswise reinforced nested circle or ellipse reinforcing structure 114, as shown in FIGURE 9. A further variation is a circular or elliptical spiral reinforcing structure 116 shown in FIGURE 10. It may be seen that the teachings of the instant invention further contemplates any nested or spiral, either connected or unconnected, configuration used for the reinforcing structure pattern.

Referring to FIGURE 11, a reinforcing structure 118 having a repeating connected honeycomb pattern is shown. Nature has shown that the honeycomb structure has superior structural integrity and strength and would therefore substantially fortify the weak dielectric layers.

It may be seen from above that the reinforcing structure may take on a variety of patterns. In general, the pattern may be regular and repeating, such as the grid, crucifix, honeycomb, and nested configurations. The pattern may also have connected or unconnected reinforcing elements. Nonrepeating patterns may also be used. The reinforcing structure pattern preferably occupies the entire or a substantial area under the bond pad and allows the weak dielectric material to fill the vacant areas between the reinforcing lines of the reinforcing structure. Further, the composition of reinforcing structure may b th same as the m talization in the corr - sponding metal layers. For example, the r inforcing structure may have a titanium nitrid /titanium nitride/titanium bottom lay r, an aluminum middle lay r, and a titanium nitride top layer. Reinforcing structur may also be constructed of other conductive or semiconductive materials.

It may be understood that the reinforcing structure of the instant invention is applicable to strengthen any bond pad with und rlying w ak dielectric layers so that it may withstand stresses and forces imparted during any wire, solder, or other bonding processes, such as flip-chip bonding, ultrasonic bonding, thermosonic bonding, thermocompression bonding, solder bump or said bump bondings, and pre-bonding wafer probe operation.

Accordingly, the teachings of the present invention includes any structure constructed substantially within the bond pad that mechanically reinforces the underlying brittle and/or soft dielectric structures. It is particularly advantageous when the reinforcing structure is comprised of an existing layer that already goes through patterning, such as the interconnecting metal lines.

Although several embodiments of the present invention and its advantages have been described in detail, it should be understood that mutations, changes, substitutions, transformations, modifications, variations, and alterations can be made therein without departing from the teachings of the present invention, the spirit and scope of the invention being set forth by the appended claims.

Claims

1. A reinforcing system for a bond pad comprising:

   at least one dielectric layer disposed under the bond pad; and
   a patterned reinforcing structure disposed in the at least one dielectric layer.

2. The reinforcing system, as set forth in Claim 1, wherein the at least one dielectric layer includes a weak organic dielectric layer.

3. The reinforcing system, as set forth in Claim 1 or Claim 2, wherein the patterned reinforcing structur is constructed of reinforcing lines of a material stronger than the dielectric layer.

4. The reinforcing system, as set forth in any of Claims 1 to 3, wherein the patterned reinforcing structure is constructed of interconnecting metalization lines.

5. The reinforcing system, as set forth in claim 1, wherein the at least one dielectric layer is at least one multi-layered dielectric stack.

6. The r inforcing system, as set forth in any of Claims 1 to 5, wh r in th patt rned reinforcing structur occupi s a substantial area under th bond pad.

7. The reinforcing system, as set forth in any of Claims 1 to 6, wherein the patterned reinforcing structure includes vacant areas filled by the dielectric layer.

8. The reinforcing system, as set forth in any of Claims 1 to 7, wherein the patterned reinforcing structure includes a grid pattern.

9. The reinforcing system, as set forth in any of Claims 1 to 7, wherein the patterned reinforcing structure includes a repeating crucifix pattern.

10. The reinforcing system, as set forth in any of Claims 1 to 7, wherein the patterned reinforcing structure includes a honeycomb pattern.

11. The reinforcing system, as set forth in any of Claims 1 to 10, wherein the patterned reinforcing structure includes alternating layers having parallel lines oriented generally perpendicularly with one another.

12. The reinforcing system, as set forth in any of Claims 1 to 11, wherein the patterned reinforcing structure includes a plurality of connected structural elements.

13. The reinforcing system, as set forth in any of Claims 1 to 12, wherein the patterned reinforcing structure includes a plurality of repeating structural elements.

14. The reinforcing system, as set forth in claim 1, wherein the patterned reinforcing structure includes a plurality of repeating non-interconnected structural elements.

15. A bond pad reinforcing system comprising:

a dielectric stack disposed under a bond pad; and

a metal reinforcing patterned structure disposed in the dielectric stack.

16. The reinforcing system, as set forth in claim 15, wherein the dielectric stack comprises multiple dielectric layers with the metal patterned reinforcing structure disposed in at least one dielectric layer therein.

17. The reinforcing system, as set forth in Claim 15 or 16, wherein the patterned reinforcing structure includes a repeating interconnected pattern.

18. The reinforcing system, as set forth in any of Claims 15 to 17, wherein the patterned reinforcing structure includes a repeating non-interconnected pattern.

19. The reinforcing system, as set forth in any of Claims 15 to 18, wherein the patterned reinforcing structure includes a plurality of nested patterns.

20. The reinforcing system, as set forth in any of Claims 15 to 18, wherein the patterned reinforcing structure includes a spiral pattern.

21. The reinforcing system, as set forth in any of Claims 15 to 20, wherein the patterned reinforcing structure includes alternating layers having parallel lines oriented generally perpendicularly with one another.

22. A method for reinforcing a bond pad in a semiconductor integrated circuit, comprising the steps of:

forming a reinforcing layer;

patterning the reinforcing layer in a predetermined area into a predetermined pattern having a plurality of vacant areas;

forming a dielectric layer above the patterned reinforcing layer, and filling the vacant areas therein; and

forming a bond pad on the dielectric layer above the patterned reinforcing layer.

23. The method, as set forth in claim 22, wherein the step of forming dielectric layer comprises the steps of forming a weak dielectric layer.

24. The method, as set forth in Claim 22 or 23, wherein the patterning step comprises the step of patterning the reinforcing layer with a repeating and interconnected pattern.

25. The method, as set forth in Claim 22 or 23, wherein the patterning step comprises the step of patterning the reinforcing layer with a repeating and non-interconnected pattern.

26. The method, as set forth in any of Claims 22 to 25, wherein the patterning step comprises the step of patterning the reinforcing layer with a nested configuration.

27. The method, as set forth in any of Claims 22 to 26, further comprising the step of repeating the reinforcing layer forming, patterning, and dielectric layer forming steps at least one time prior to forming the bond pad thereon.

FIG. 1

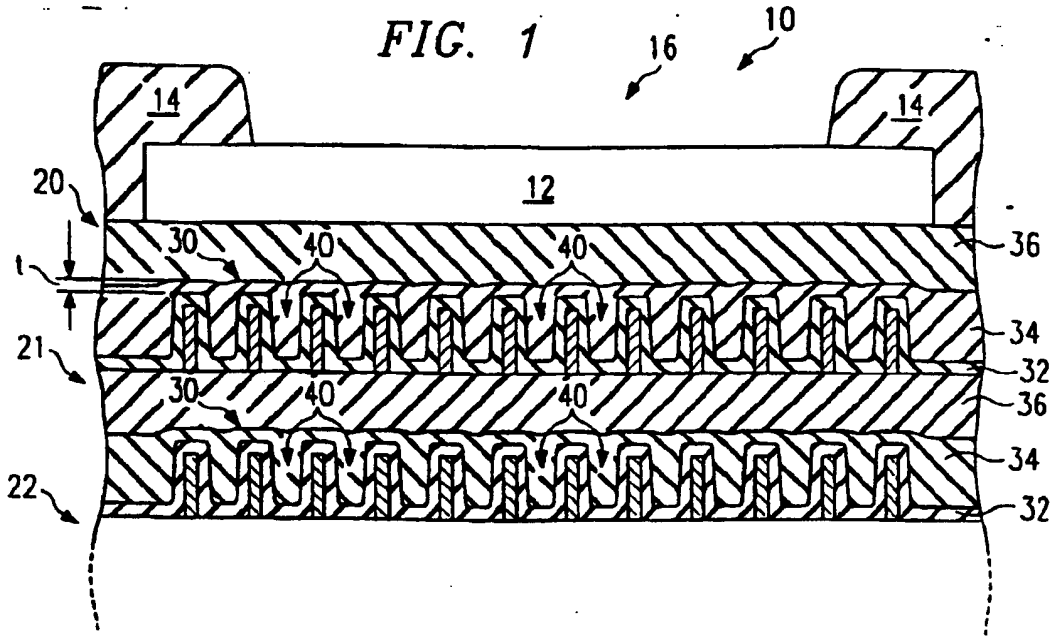


FIG. 2

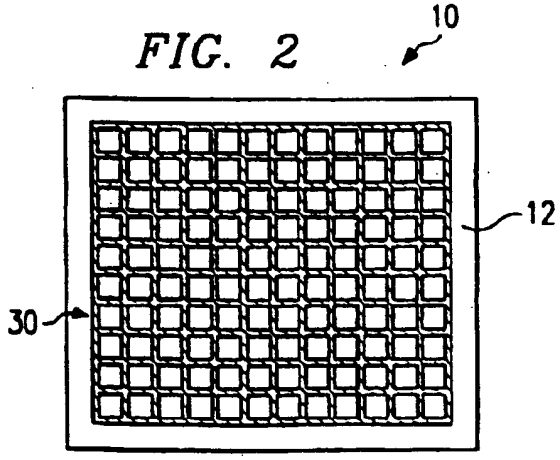


FIG. 4A

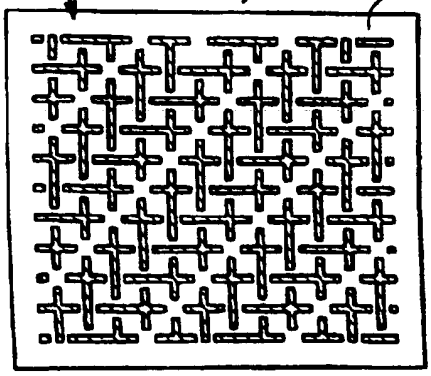


FIG. 4B

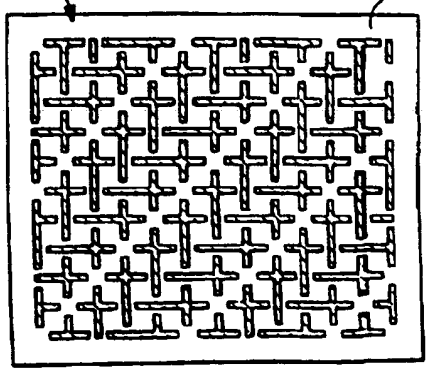


FIG. 3

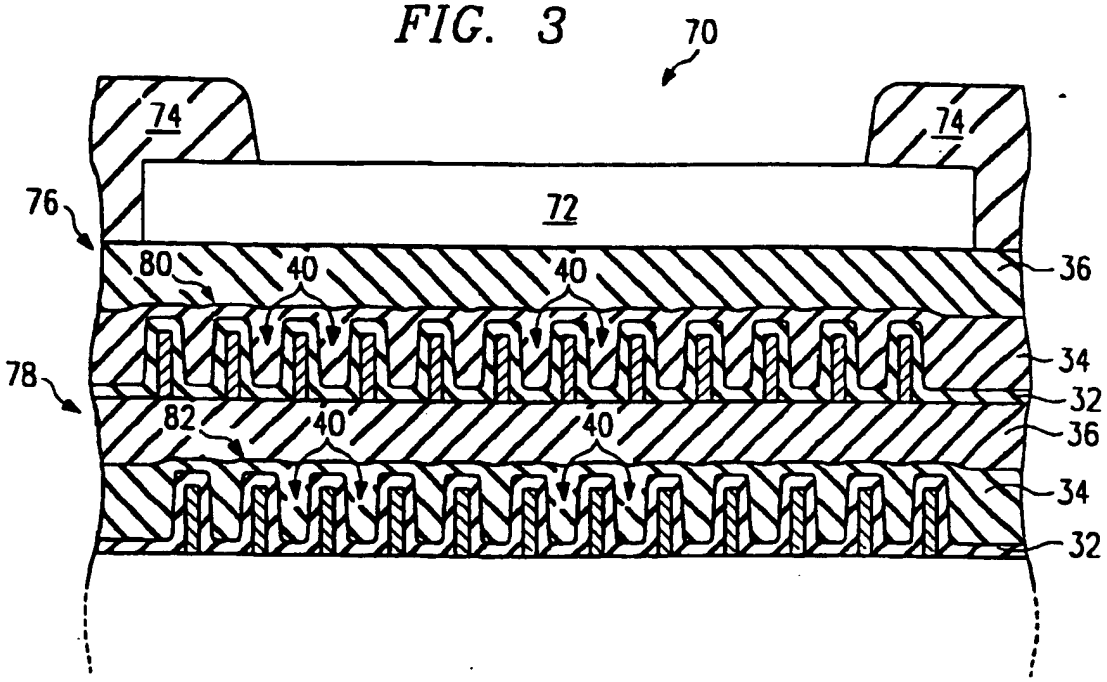

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FIG. 5

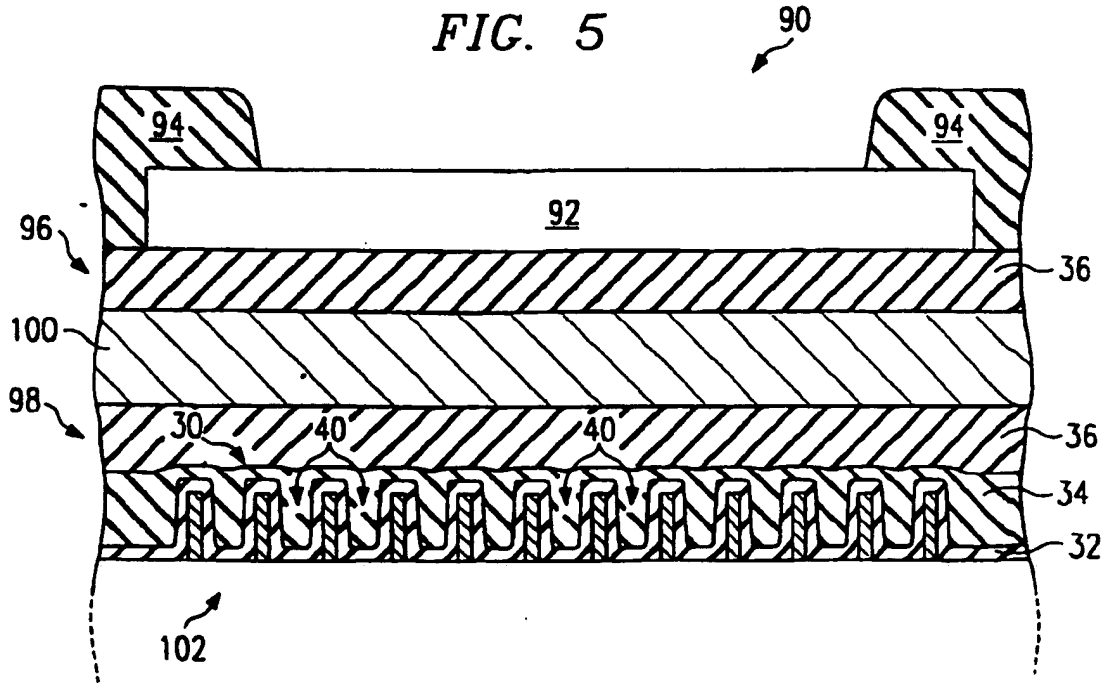
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FIG. 6

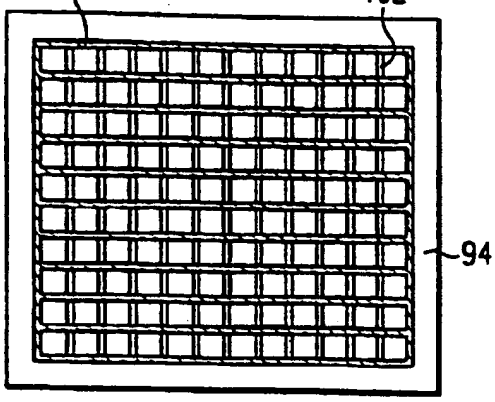

FIG. 7

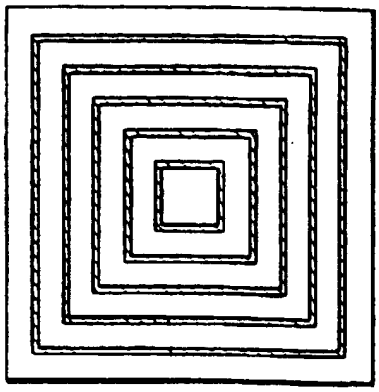

FIG. 8

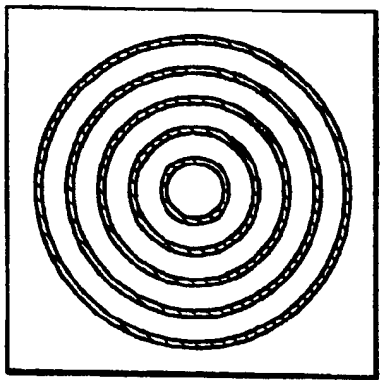

FIG. 9

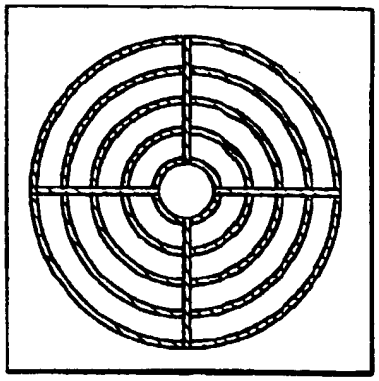

FIG. 10

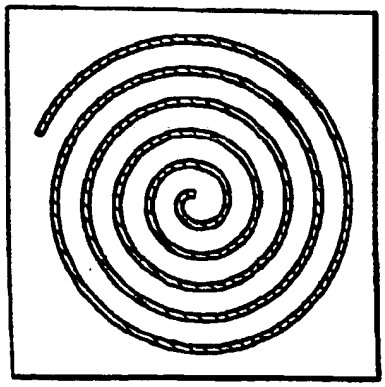

FIG. 11

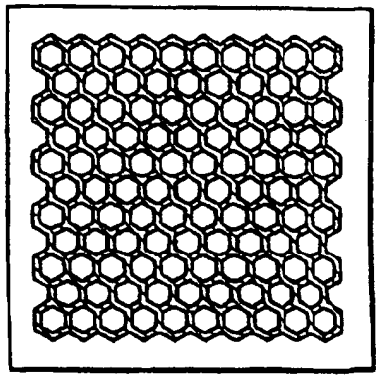

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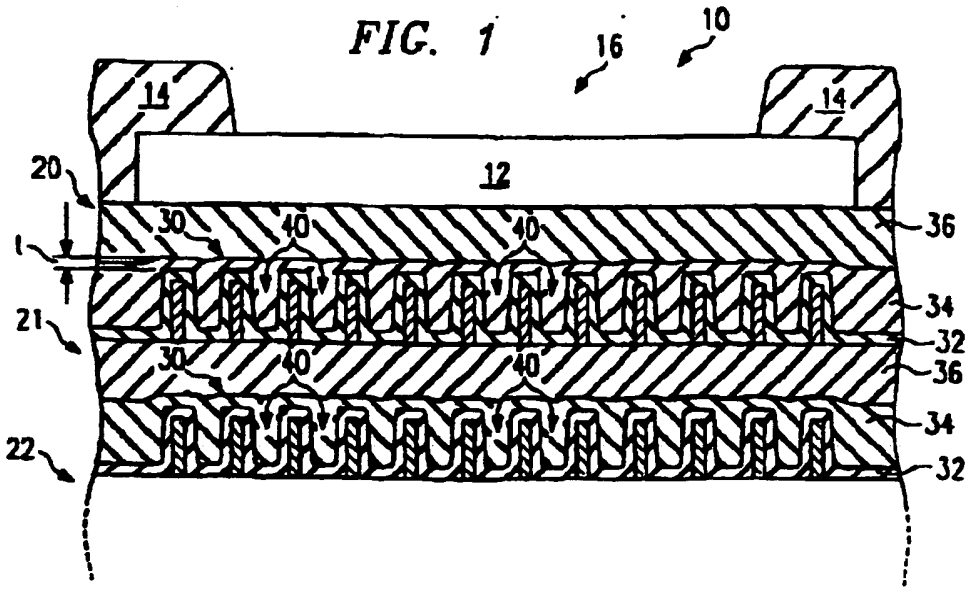
FIG. 1



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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 30 3365

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 340 727 A (NIPPON ELECTRIC CO) 8 November 1989 (1989-11-08) * figures 2A,2B,4A,4B,5 * * column 1, line 43 - line 49 * * column 6, line 36 - line 42 * * column 8, line 9 - line 25 * * column 8, line 50 - line 54 *	1-21	H01L23/48 H01L23/498 H05K1/02
A	---	23-27	
X	US 5 288 661 A (SATOH SHINICHI ET AL) 22 February 1994 (1994-02-22) * figures 1A,3A,4A-4C,4F,4G,5-7 * * column 4, line 55 - column 5, line 13 * * column 6, line 24 - column 7, line 10 *	1,3,6, 15,22,23	
Y	---	4,16-21, 24-27	
X	PATENT ABSTRACTS OF JAPAN vol. 014, no. 168 (E-0912), 30 March 1990 (1990-03-30) -& JP 02 026039 A (MITSUBISHI ELECTRIC CORP), 29 January 1990 (1990-01-29) * abstract; figures 1-3 * * page 205, column 2, line 15 *	1,3,5-14	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L H05K
Y	---	4,16-21, 24-27	
	-/--		

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	16 August 1999	Polesello, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
P,X	SARAN M ET AL: "Elimination of bond-pad damage through structural reinforcement of intermetal dielectrics" 1998 IEEE INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM PROCEEDINGS. 36TH ANNUAL (CAT. NO.98CH36173), 1998 IEEE INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM PROCEEDINGS 36TH ANNUAL, RENO, NV, USA, 31 MARCH-2 APRIL 1998, pages 225-231, XP002112247 1998, New York, NY, USA, IEEE, USAISBN: 0-7803-4400-6 * page 226, column 2, line 35 - page 227, column 2, line 2; figures 6-8; table 1 *	1-27	
P,X	US 5 703 408 A (WU DER-YUAN ET AL) 30 December 1997 (1997-12-30) * figures 3-7 * * column 3, line 20 - line 57 * * column 4, line 11 - line 32 *	1,5-7, 13-16, 18,19	
P,A		22,23, 25,26	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
A	PATENT ABSTRACTS OF JAPAN vol. 013, no. 280 (E-779), 27 June 1989 (1989-06-27) -& JP 01 065895 A (HITACHI CABLE LTD), 13 March 1989 (1989-03-13) * abstract *	1,3,4, 6-8,12, 13,15, 17,22-24	
A	EP 0 244 699 A (MITSUBISHI PLASTICS IND) 11 November 1987 (1987-11-11) * figures 1-3 * * page 5, line 6 - line 25 * * page 6, line 10 - line 15 *	1-4,6-8, 12,13, 15,17, 22-24,27	

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	16 August 1999	Polesello, P

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EUROPEAN SEARCH REPORT

Application Number
EP 98 30 3365

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 4 572 754 A (BLOOM TERRY R) 25 February 1986 (1986-02-25) * figures 1-4 * * column 3, line 53 - line 68 * * column 5, line 15 *	1-6,8, 11-13, 15-17,21	
A	US 5 085 922 A (MURASAWA YASUHIRO) 4 February 1992 (1992-02-04) * figures 14,15 * * column 3, line 23 - line 51 *	1-3,5-8, 11-13	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	16 August 1999	Polesello, P

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X : particularly relevant if taken alone
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16-08-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0340727 A	08-11-1989	JP 1280337 A	10-11-1989
		JP 2062857 C	24-06-1996
		JP 7097602 B	18-10-1995
		DE 68918983 D	01-12-1994
		DE 68918983 T	01-06-1995
		US 5124781 A	23-06-1992
US 5288661 A	22-02-1994	JP 2598328 B	09-04-1997
		JP 3131044 A	04-06-1991
		DE 4019848 A	25-04-1991
		US 5084752 A	28-01-1992
JP 02026039 A	29-01-1990	NONE	
US 5703408 A	30-12-1997	US 5834365 A	10-11-1998
JP 01065895 A	13-03-1989	NONE	
EP 0244699 A	11-11-1987	JP 1854387 C	07-07-1994
		JP 5074457 B	18-10-1993
		JP 62251136 A	31-10-1987
		DE 3784760 A	22-04-1993
		DE 3784760 T	21-10-1993
		US 4769270 A	06-09-1988
US 4572754 A	25-02-1986	US 4689262 A	25-08-1987
US 5085922 A	04-02-1992	NONE	

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82